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Report 10

Quarterly Progress Report 10 | *Covering the Period 1 September 1962 to 30 November 1962*

GRAPHICAL DATA PROCESSING RESEARCH STUDY AND EXPERIMENTAL INVESTIGATION

Prepared for:

U.S. ARMY SIGNAL RESEARCH AND DEVELOPMENT LABORATORY
FORT MONMOUTH, NEW JERSEY

CONTRACT DA 36-039 SC-78343
SCL 4087 (18 NOVEMBER 1958)
FILE NO. 40001-PM-60-91-91(6500)
DA PROJECT 3A99-22-001-02

By: *A. E. Brain* *H. S. Crafts* *G. E. Forsen* *D. J. Hall*
J. W. Machanik

STANFORD RESEARCH INSTITUTE

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SRI Project No. 3192

Objective: To conduct a research study and experimental investigation of techniques and equipment characteristics of pattern recognition systems suitable for practical application to graphical data processing for military requirements.

Approved:

C. A. ROSEN, MANAGER APPLIED PHYSICS LABORATORY

J. E. NOE, DIRECTOR ENGINEERING SCIENCES DIVISION

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PURPOSE

It is the objective of this project to conduct a research study and experimental investigation of techniques and equipment characteristics suitable for practical application to non-alphanumeric graphical data processing for military requirements. All phases of the graphical data processing art will be considered, including the treatment of raw graphical data, identification, programming, selection, indexing, access to storage, and presentation. The studies and demonstrations of feasibility will be designed to evaluate the practicability of the proposed techniques and systems, with sufficient detail to be useful in establishing the design criteria necessary for equipment procurement.

The program of work to be carried out in accordance with the extension of Contract DA 36-039 SC-78343 will consist of:

(1) The study and development of organizations of combined fixed and adaptive networks that will permit recognition of patterns independent of size, displacement, and rotation, (a) in the presence of interfering signals and noise, and (b) on a real-time basis.

(2) The development of components and subsystems suitable for implementing the schemes devised in (1).

(3) The design and construction of an experimental Graphical Data Processing Machine making use of the techniques and components found to be most practicable by investigations (1) and (2).

ABSTRACT

Major decisions have been made regarding the design of the experimental pattern-recognition machine, MINOS II, to be constructed under the present contract. Much of the total effort has been expended in support of our fundamental premise that the development of inexpensive, adaptive weights will allow their use in quantities sufficient to ensure the practicality of learning machines for real pattern-recognition tasks. Several devices dependent on the electromagnetic or magnetostrictive properties of common magnetic materials or components have been developed and are described. All are compatible with some form of coordinate-address logic for nondestructive read-out and adaptation. Two sonic transmission-line configurations allow the use of time-dependent logic if needed. Several multiaperture ferrite core configurations offer high reliability and speed. An adaptive weight with desirable storage characteristics, invented by H. S. Crafts (now an SRI staff member), was re-examined as a result of a substantial reduction in component cost. This weight uses two tape-wound cores which generate a second-harmonic component proportional to the net remanent flux when driven by a high-frequency current. The above features, combined with the development at SRI by Crafts and G. E. Forsen of a simple coordinate-address array, determined the choice of this weight for MINOS II.

System simulation studies pertinent to the design of MINOS II are summarized. It was determined that majority-rule coding of the binary outputs of a layer of adaptive, threshold-logic units compares favorably, for random input patterns, with maximal-length, shift-register coding, and is simpler to use from a hardware point of view. System and circuitry design requirements and realizations for the preprocessing unit of MINOS II are also described.

PUBLICATIONS, LECTURES, REPORTS, AND CONFERENCES

An article written by A. E. Brain, G. E. Forsen, N. J. Nilsson, and C. A. Rosen entitled "Learning Machines," appeared in the November issue of International Science and Technology.

Professors Frank Rosenblatt and David Block, of Cornell University, visited SRI in October to discuss system design and preprocessors for automatic feature-extraction. Dr. George Nagy, also of Cornell, worked at SRI evaluating components appropriate for the pattern recognition machine under construction at Cornell.

I INTRODUCTION: SOME MAJOR DECISIONS REGARDING THE CONSTRUCTION OF MINOS II

Several major decisions have now been made, affecting the basic components and design of the experimental machine to be constructed under the present contract. The implementation of these decisions in terms of hardware has already begun.

In line with our fundamental premise that the future practical application of learning machines is closely tied to the development of inexpensive weights and their use in large quantities, a substantial part of our effort has been devoted to the search for devices having the desired characteristics. The behavior of some of the devices investigated is surveyed in Sec. II.

It should be noted that each of the devices described is potentially capable of forming the central component of a learning machine system, and that the spread in the cost per weight is not large--probably less than 5:1, depending on the ingenuity and development put into the mechanical and electrical design. For conditions outside the boundaries set by the present application, other components described in this report may possess auxiliary properties so desirable as to justify their slightly higher basic cost. Thus, if time-dependent logic is needed, one of the delay-line configurations might be compatible with the required sequential processing. As another example, a circuit using a multiaperture core for the weight and a small memory core for the increment-decrement logic would have high resistance to extraneous electrical interference.

However, the circuit having the lowest average cost per weight is the arrangement described in Sec. III, where a wired-up, completed plane of several hundred weights is considered. The other devices do not lend themselves fully to "push-through" wiring, and consequently require the use of from two to five connecting pins per weight. There is thus a substantial labor cost for stripping the fine wire and making the connections.

It now appears possible to fabricate planes for a cost in the neighborhood of $1.50 per weight, including cores but excluding drivers. On this basis, it has been decided to build the variable-weight part of the machine at full scale, which means 6600 weights. This number is a natural result of previous (arbitrary) decisions: initially it was decided to classify the input patterns into 64 categories, and to preprocess the raw data to provide a 100-bit code word as input for the variable-weight part of the machine. An "everything-to-everything" type of wiring between the 100 input lines and the association units is highly desirable. The 64 output categories may be created from 63 association units by the matched-filter technique described in Quarterly Progress Reports 8 and 9, or by using six one-bit machines in parallel, where each output bit is derived from the majority vote of eleven association units. The latter arrangement calls for 6600 weights. Since majority-vote logic is simpler to implement, and, as shown by the simulations described in Sec. IV, is competitive in performance, MINOS II will be wired up initially as six parallel one-bit machines. This arrangement will probably be somewhat easier than any other to trouble-shoot.

Section V contains a description of the circuitry and design parameters associated with the optical preprocessor and the output display panel. Construction of this part of the hardware for MINOS II is making good progress.

II A SUMMARY OF OUR EXPERIENCES ON THE PRACTICAL PERFORMANCE OF VARIOUS TYPES OF MAGNETIC WEIGHT

A. BACKGROUND

This section reviews several of the magnetic weighting schemes investigated, explains the "ground rules" of the investigation, and summarizes the criteria used in the evaluation.

It has been basic to our philosophy that future practical applications will require machines having very large numbers of weights. We are dealing with statistical behavior and, in order to achieve tolerable error rates (say < 1%), it will be necessary to work with systems having as many as 10^4 weights, or more. Systems utilizing 10^6 weights can readily be envisaged. In order that such machines may be built, our short-term goal must be to produce a weight and its associated circuitry for about a dollar; over a long period, this cost might very well have to be reduced to 10 cents.

Neither environmental stability nor high reading speed can be sacrificed to lower costs. We might forego a certain amount of linearity, as long as the device does not drift or degrade on read-out and can be set with reasonable accuracy. What is reasonable? Simulated experiments can give us a lead: In one of our simulations of majority logic, with 400 patterns in a training sequence and 400 weights per bit of the output code, convergence was obtained for all four bits of the output code after 29 iterations. The largest positive weight was 53, the largest negative weight was 39. This simulation may be considered typical of the kind of numbers likely to arise in practical applications. Thus, a setting accuracy of 1 part in 100 over the storage range appears to be more than adequate for a component that is sufficiently stable. In practice, saturation of a small proportion of the weights is unlikely to be seriously detrimental.

On the basis of these parameters it was early concluded that devices based on magnetic storage in square-loop materials showed most promise

of providing the desired characteristics, and our efforts have been concentrated in this direction. For other boundary conditions, it is possible that other devices may be competitive, or may even confer highly desirable benefits. Our purpose here is to render an account of some of the potentially usable devices that have been investigated. It is worth noting that each of the arrangements described is sufficiently practical to form the basis for a machine, and that factors other than those already discussed may be important for particular applications; for example, there might be a need for time-dependent logic. Since our production cost for these devices lies in a range of only about 5 to 1, a little ingenuity in fabrication techniques might render any one of them competitive.

B. CIRCUIT BASED ON TWO MULTIAPERTURE CORES

The circuit used for the magnetic weights in MINOS I is shown in Fig. 1. Although this arrangement is electrically adequate, too much winding time was required in the production of the complicated gate core.

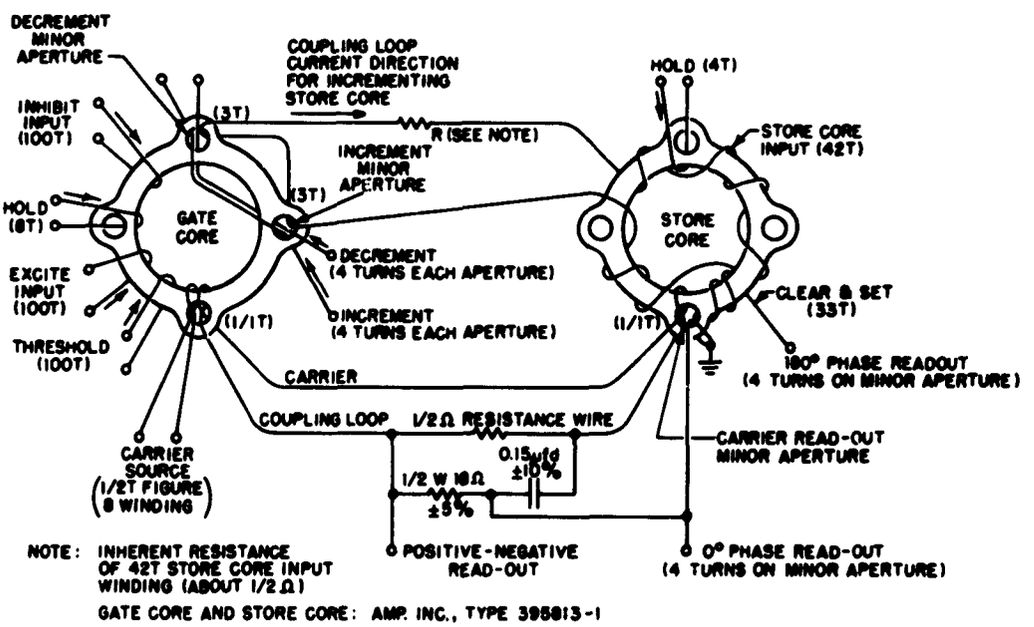


FIG. 1 CIRCUIT BASED ON TWO MULTIAPERTURE CORES AND USED IN MINOS I

Since the very small minor apertures cannot be wound by machine, there seemed to be no prospect of cutting the cost to one dollar per weight--the goal we had set as representing the level at which the construction of large machines becomes economical. No attempt has been made to develop this circuit further (see Quarterly Progress Reports 1, 3, and 4 on this project).

C. ACOUSTICAL WIRE DELAY LINE

This arrangement, shown in Fig. 2, was described in Quarterly Progress Report 5. It has two disadvantages: (1) the demagnetizing effects are such that a length-to-diameter ratio of about 200:1 is needed in order to retain a sufficiently square hysteresis loop; and (2) there appeared to be no simple scheme for weight changing. However, our later experience

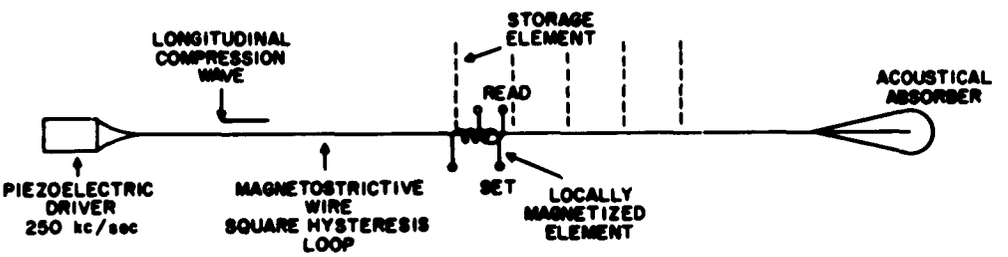


FIG. 2 ACOUSTICAL WIRE DELAY LINE HAVING MULTIPLE MAGNETIC WEIGHTS

with the bucket-core logic technique described in Quarterly Progress Report 9 is probably applicable here. Several variants of the wire technique were tried, including the use of electroplated thin films of 80-20 Ni-Fe; this gave an appreciable improvement in combating demagnetizing effects. Even so, more promising results were obtained using memory cores.

D. MEMORY TOROIDS ON A DELAY LINE

This technique was described at some length in Quarterly Progress Reports 7 and 9 (see also Figs. 3, 4, and 5). The logic necessary for

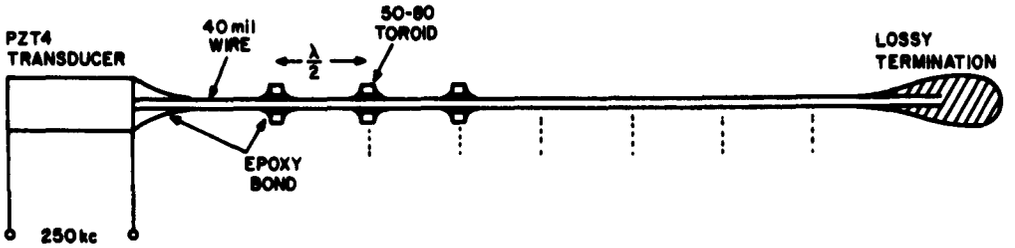


FIG. 3 DELAY LINE HAVING MULTIPLE WEIGHTS IN THE FORM OF MAGNETOSTRICTIVE FERRITE TOROIDS

weight-changing is obtained compatibly by using an auxiliary array of memory cores; it is possible for (m + n) drivers to control (m x n) weights.

Manufacturers were not enthusiastic about undertaking the construction of delay lines for MINOS II. The use of metered amounts of epoxy cement is not a standard practice; the "potentiometer" wind of 20 turns of fine wire in a 50-80 memory core (by hand) is expensive; and a large number of connections must be made to fine wires. It seemed unlikely that anyone could make a weight-gate pair, exclusive of drivers, for a manufacturing cost much below $3.00.

At this stage, it became necessary to reconsider the weights to be used in MINOS II. We were reluctant to use fewer than 6600 weights, since lesser numbers do not permit the same flexibility in machine organization; at the same time, the possibility of using the time-dependent logic made available by the nature of the delay-line structure seemed distant, especially in the light of the contractual requirement to deliver hardware in six months. Thus, further experimental work was begun, to see whether some more desirable proposition had been overlooked--in particular, one that would require less hand labor in manufacture.

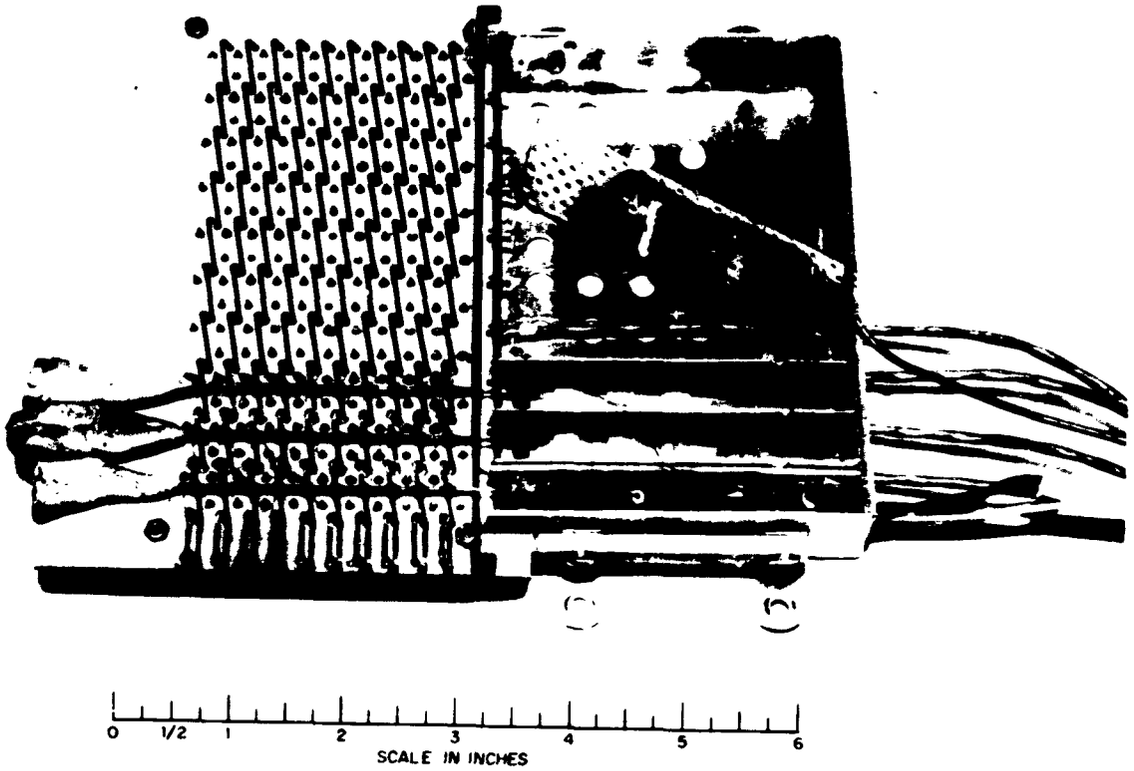


FIG. 4 DELAY-LINE MODULE, PARTIALLY ASSEMBLED

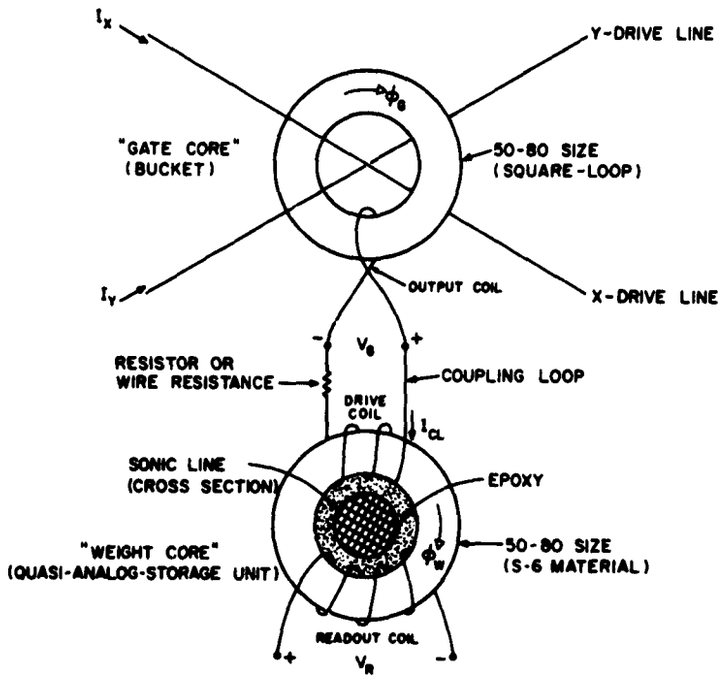


FIG. 5 FERRITE TOROID (Weight-Gate) PAIR

E. SIMPLIFIED MULTIAPERTURE CORE CIRCUITS

The main defect of the circuit used for MINOS I lay in the complication of the gate core. A satisfactory increment-decrement scheme based on single-toroid logic had already been demonstrated for use with toroids on a delay line; it was determined that this could be applied directly for changing weights stored in multiaperture cores. The simplified arrangement and a counting curve is shown in Fig. 6. This circuit deserves consideration for applications where there is possibility of disturbances from powerful switching transients in adjacent equipment. The bucket core of S4 material has a very high threshold, a very square loop, and is driven by single-turn wiring; the coupling loop has minimum area; thus it is difficult to modify the stored value via the carrier drive and read-out windings.

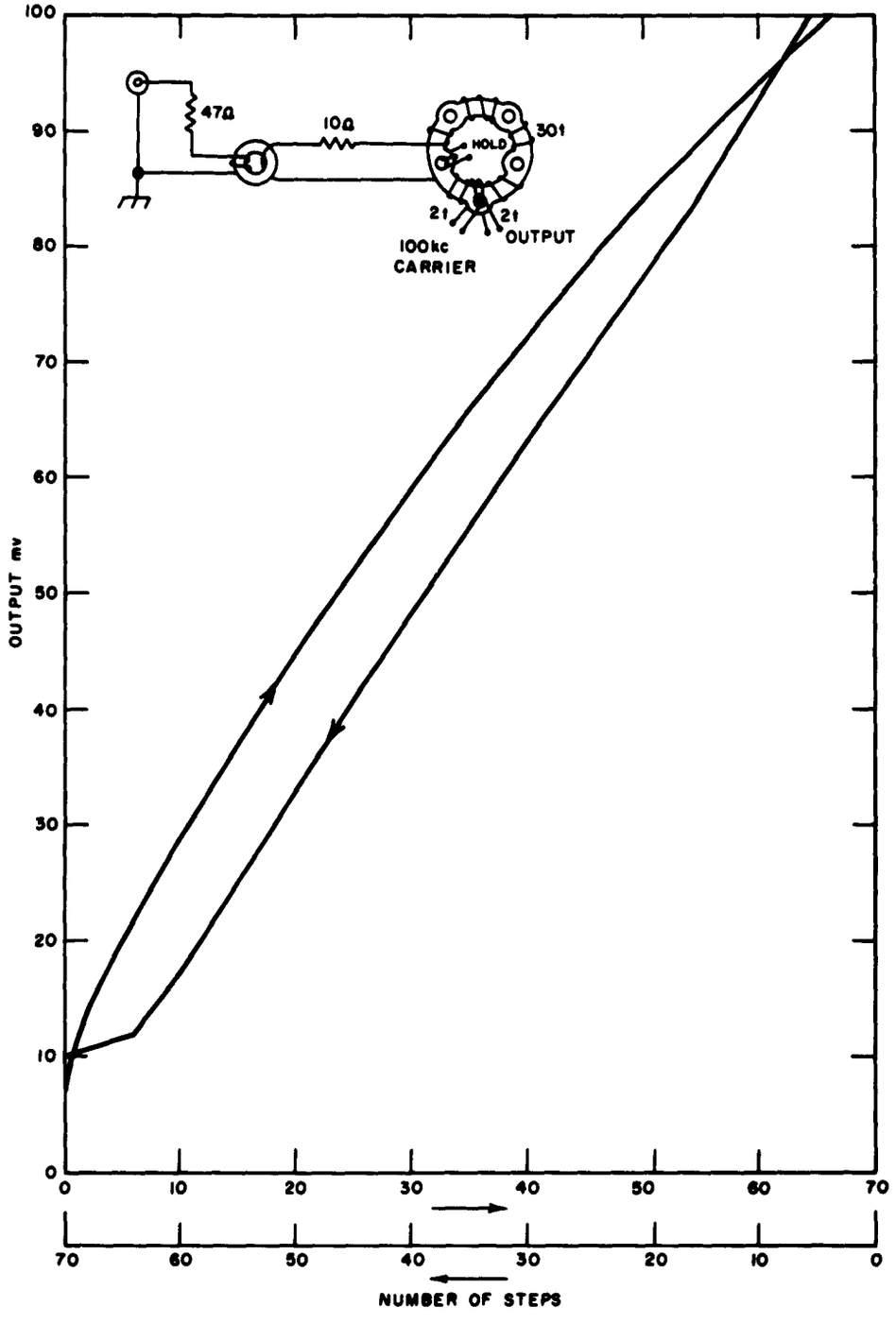


FIG. 6 CIRCUIT USING A MULTIAPERTURE CORE FOR THE WEIGHT AND A TOROID FOR THE INCREMENT-DECREMENT LOGIC AND ITS STORAGE CHARACTERISTIC

It is worth noting that an improved multiaperture core, AMP type, SCO-001-1, is available in production quantities, and it is shown in Fig. 6. It has a prescribed read-out aperture, where the total cross section of the core is a minimum, and consequently gives a low minimum output when the core is driven into saturation in one direction over the whole of its cross section. (For MINOS I the read-out apertures were enlarged with an ultrasonic drill.)

The circuit can be reduced even further by eliminating the bucket core, and by putting into the store winding a carrier along with a low-level increment-decrement pulse (see Sec. III); this arrangement (Fig. 7) was tested with 30 turns on the store winding. It was assumed that single-turn coincident-current carrier-pulse drive would also be applicable and a similar circuit, based on coincident-current, pulse-only logic, using single-turn, straight-through windings which was briefly investigated, appeared promising. A possible, single-turn, physical layout appears in Fig. 8.

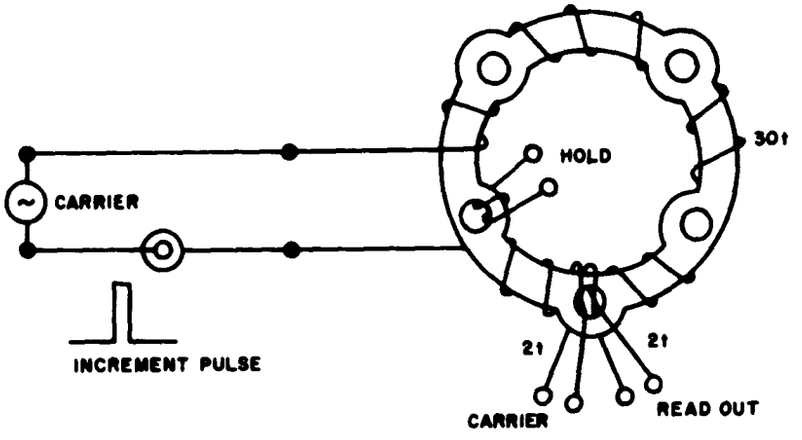
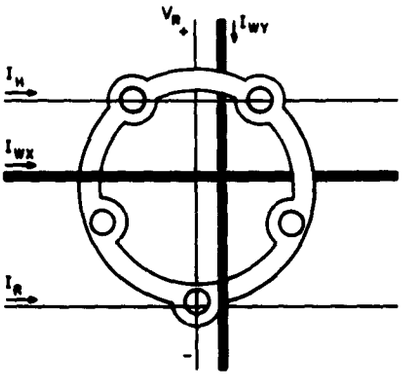


FIG. 7 CIRCUIT USING MULTIAPERTURE CORE FOR THE WEIGHT, AND THE SQUARE-LOOP PROPERTIES OF ITS OWN MAJOR APERTURE FOR INCREMENT-DECREMENT LOGIC



KEY

I_H = HOLD CURRENT (DC)
I_R = READ CURRENT (PULSE)
I_{WX} = WRITE CURRENT X (PULSE/CARRIER)
I_{WY} = WRITE CURRENT Y (PULSE)
V_R = READ-OUT VOLTAGE

FIG. 8 SINGLE-TURN CIRCUIT USING MULTIAPERTURE CORE FOR THE WEIGHT, AND THE SQUARE-LOOP PROPERTIES OF ITS OWN MAJOR APERTURE FOR COINCIDENT-CURRENT ADAPTATION LOGIC

These experimental circuits have not been pursued further, since an alternative method based on tape-wound cores and second-harmonic read-out, which was being tested at the same time, gave good enough results to warrant its use for MINOS II.

F. CIRCUIT BASED ON SECOND-HARMONIC READ-OUT FROM PARTIALLY-SET TAPE-WOUND CORES

This arrangement (Fig. 9) consists of a pair of tape-wound cores that are driven from a high-frequency, pure sinusoidal power source. The windings are so arranged that the fundamental component of the voltage induced in each core cancels out, leaving a second harmonic distortion voltage that is proportional to the remanent flux in the core(s). The configuration of cores and wiring is extremely simple; it lends itself readily to manufacture, and the electrical performance is entirely adequate. A detailed account of this arrangement is given in Sec. III.

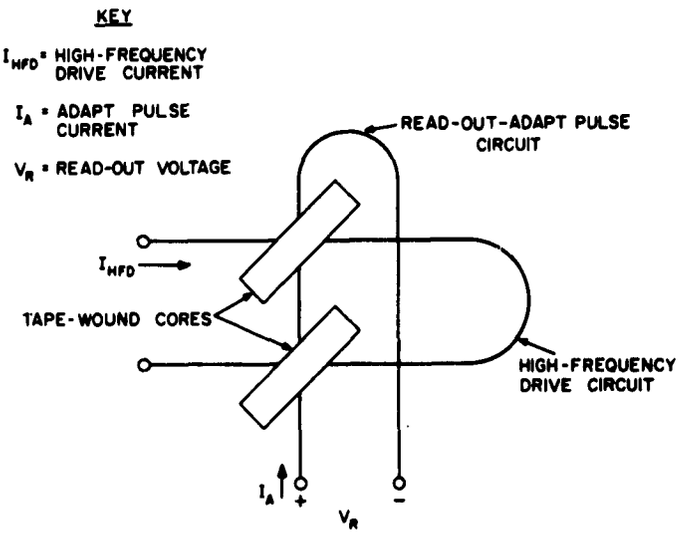


FIG. 9 BASIC TAPE-WOUND CORE-PAIR WEIGHT CIRCUIT

G. CONCLUSIONS

For the present application, the method using second-harmonic read-out from tape-wound cores is most promising and will be used as the basis for MINOS II.

III THE TAPE-WOUND, CORE-PAIR WEIGHT ARRAY FOR MINOS II

A. SUMMARY

A substantial reduction in price in certain tape-wound cores created renewed interest in a new weight realization. An analog storage unit was invented under Contract AF 33(616)-7726 at Stanford University by Harold Crafts (now employed by Stanford Research Institute), which uses two tape-wound, nickel-iron alloy, square-loop cores (see Fig. 9). The cores are electrically driven by a high-frequency current in opposite senses. The outputs of both cores are summed in the same sense, thereby cancelling the fundamental and leaving mostly even harmonics. The second harmonic was found to be proportional to the remanent magnetic state of the cores. The analog value, stored as the net amount of remanent flux, is read out nondestructively with the application of a sufficiently small, high-frequency, drive current. The tape-wound core is more linear than the magnetostrictive ferrite-core realization, exhibits a larger number of usable levels, and produces more output signal. The rectangular matrix array concept of organization, invented for the ferrite-core weight (Quarterly Progress Report 9) was successfully applied to the tape-wound core weight by making use of the latter's adaptation threshold properties. The ability to read out nondestructively, or to change the stored value of any single weight or any concommitant combination of weights in an (m x n) array using (m + n) coordinate address signals greatly enhances the economy of system construction and operation.

Quotations on this new matrix-array of tape-wound cores have resulted in our lowest unit cost to date, around $1.50.

B. THE TAPE-WOUND, CORE-PAIR WEIGHT

It has been found[1*] that by driving a one-mil, 200-Maxwell, tape-wound core with a high-frequency current (e.g., 100 kc) whose period is

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*References are listed at the end of the report.

shorter than the nominal switching time, the direct-current threshold of these "square-loop" cores may be exceeded by a factor of two to three without noticeably altering the remanent flux state. It was also found that the remanent flux state could be changed by the combination of the high-frequency current and a direct current bias, neither of which could, by itself, switch any flux permanently. The voltage developed at the winding terminals when the cores are driven by current sources has considerable harmonic content. The magnitude of the fundamental frequency component of this voltage is a relatively insensitive and nonlinear function of the remanent flux state, but the second harmonic component is a sensitive and apparently linear function of the remanent state. Thus the state of the core can be read out nondestructively by measuring the second harmonic voltage, whose amplitude and phase determine the amount and direction (respectively) of the net remanent flux in the core.

While a single core can be used as a weight,* considerable filtering is needed to remove the fundamental from the read-out circuitry and the second harmonic from the drive circuitry. For a system of the dimensions planned for MINOS II, it was deemed expedient to use two cores per weight. The two cores are driven by the high-frequency current in opposing senses, and the read-out voltage of each is summed in the same sense. This tends to cancel the fundamental component in the read-out voltage, and also the second harmonic component in the drive current. The extent of the cancellation depends on the manufacturer's quality control. Tests to date indicate that uniformity is sufficient to require no more than capacitive tuning of the high-frequency drive circuit and one stage of L-C filtering on the read-out circuit.

C. POSSIBLE OPERATING RANGES FOR TAPE-WOUND CORE-PAIR WEIGHTS

The maximum high-frequency drive current that can be applied to the core-pair without disturbing the remanent flux state is on the order of

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*Dr. George Nagy of Cornell University worked with our group during the month of November and developed a one-core version. This arrangement may be used in the large adaptive machine (TOBERMOREY) being constructed at Cornell University under the direction of Frank Rosenblatt.

2 ampere-turns peak-to-peak; however, it has been found that a more linear storage characteristic is obtained at lower drive levels--e.g., 1.0 to 1.5 ampere-turns. Because the ratio of second harmonic to fundamental component in read-out voltage is roughly proportional to the magnitude of the high-frequency drive current, less filtering and less amplification is required in the read-out circuits at the higher drive levels. A value of 1.2 ampere-turns is felt to give a reasonable compromise between linearity and equipment complexity requirements; at this drive level, 10 millivolts (peak-to-peak) per turn of second-harmonic output voltage is obtained. The ratio of second harmonic to fundamental in the output of each core, at this drive level, is approximately 1:10, and the ratio in the summed output of the core-pair is approximately 4:1. This cancellation of the fundamental in the read-out circuit of the core-pair is equivalent to a 26-db rejection filter. The maximum direct-current bias that can be applied to the core-pair and not disturb the remanent flux state is approximately 200 milliampere-turns. The smallest usable direct-current bias (adapt current) is about 100 milliampere-turns. This gives at least a two-to-one range in permissible adapt current when requiring a coincidence of high-frequency drive current and adapt current to change the remanent flux state.

Adaptive networks of the type for which this weight is intended often change stored values by fixed amounts which are (usually small) fractions of the total range between positive and negative saturation values. Figure 10 shows the storage characteristic of a tape-wound core-pair weight selected at random from an experimental array, operated under normal conditions. Considerable controlled variation in this characteristic may be achieved by changing the amplitude of the high-frequency drive current; changing the amplitude or the duration of the adapt current (or both) provides an especially good method of controlling the change. It is easiest to control the amount of change of stored value per application of adapt current, by changing the adapt-current duration.

At given high-frequency drive-current and adapt-current levels, the rate of change of stored value is almost insensitive to the state of the

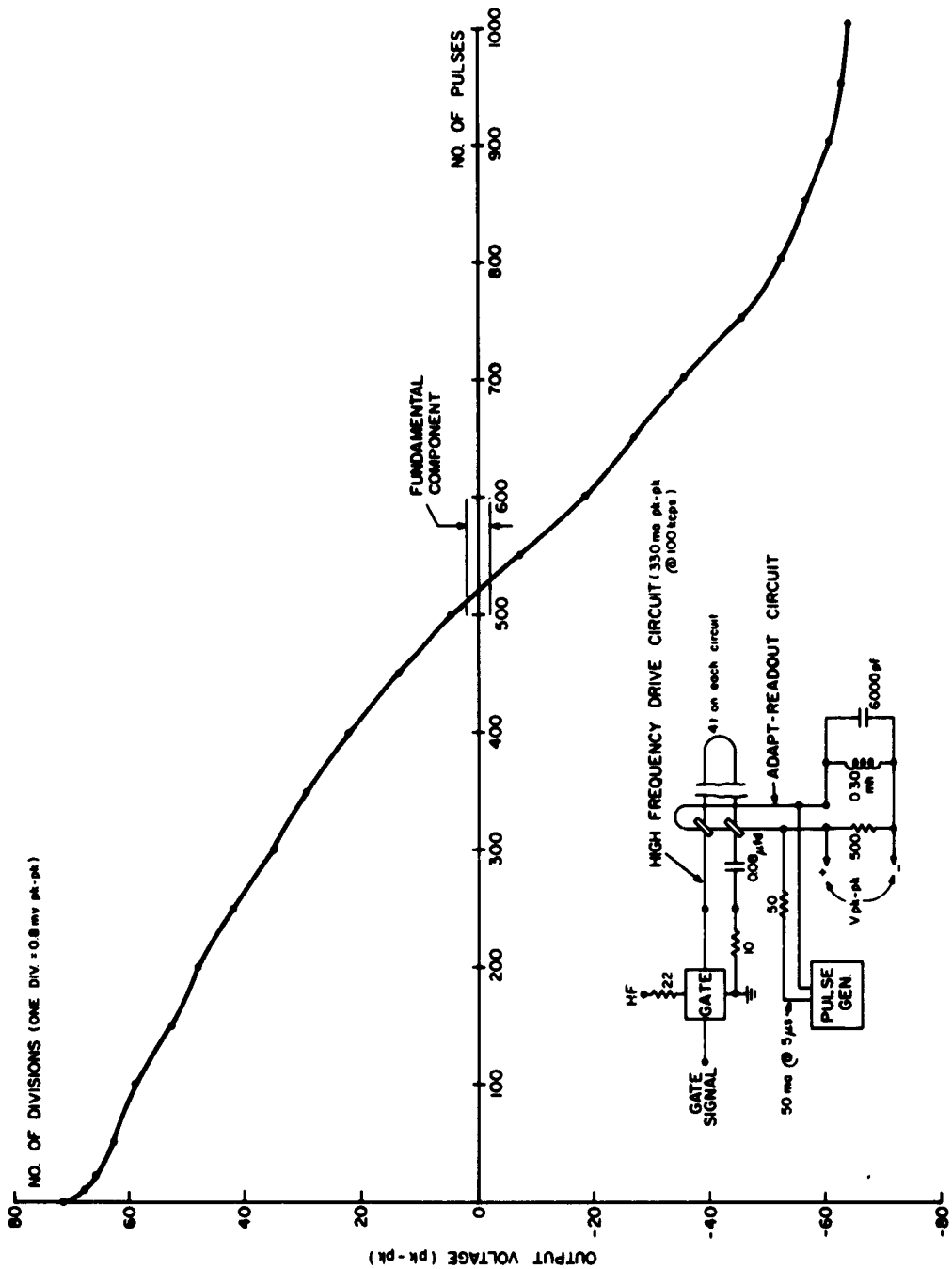


FIG. 10 STORAGE CHARACTERISTIC OF A TAPE-WOUND CORE-PAIR WEIGHT SELECTED AT RANDOM FROM AN EXPERIMENTAL MATRIX ARRAY

core and the past history of adaptation. There are two exceptions to this insensitivity which are considered minor for the present application: The rate of change is initially larger upon a reversal in sign of the adapt current, and is progressively smaller in magnitude when nearing either saturation value. (This is typical of magnetic analog-storage devices.) These exceptions may possibly assist adaptive system performance. Variable adapt-current duration (i.e., variable pulse duration) which will allow automatic regulation of the magnitudes of the increment pulses may be incorporated in MINOS II.

The number of increments in the total range may be varied from one to over one thousand merely by altering the adapt-pulse duration. However, in order to obtain one thousand increments, the adapt-pulse duration approaches a minimum value necessary for permanent switching (approximately 5 microseconds at an adapt-pulse current level of 200 milliampere-turns). More steps could be obtained by lowering the magnitude of the adapt-pulse current, but this would accentuate the existing nonlinearities in the storage characteristic.

D. THE CORE ARRAY SCHEME

The adaptation threshold properties of the Crafts weight make it possible to use a coordinate address scheme similar to that previously developed for the magnetostrictive-ferrite-toroid weight. As described above, the combination of the high-frequency drive-current and an adapt-current pulse will change the remanent flux state, while either alone will not. Thus it is possible to arrange each core-pair in a rectangular array with integer-valued Cartesian coordinates. Each core-pair (i.e., each weight) is assigned an X-coordinate and a Y-coordinate. Each of the m inputs to the array is given an X-coordinate and each of the n outputs is given a Y-coordinate. Each input circuit links, in series, n weights, and each output circuit links, in series, m weights. Thus, each output is connected via a weight to each input, and vice versa. See Fig. 11 for the corresponding physical arrangement.

Each input circuit--i.e., each X-line in the tape-wound, core-pair array--is a high-frequency drive line. It drives all n weights

associated with that particular input. This line passes through one core of the core-pair and back through the other, thus achieving the opposite-sense drive described in Sec. III-B. Each output circuit (i.e., each Y-line) is a read-out and adapt line for all m weights associated with that particular output. This line passes through both cores of the core-pair in the same sense. It sums the read-out voltages, and provides a circuit for the adapt-current pulse, for all m weights on that line.

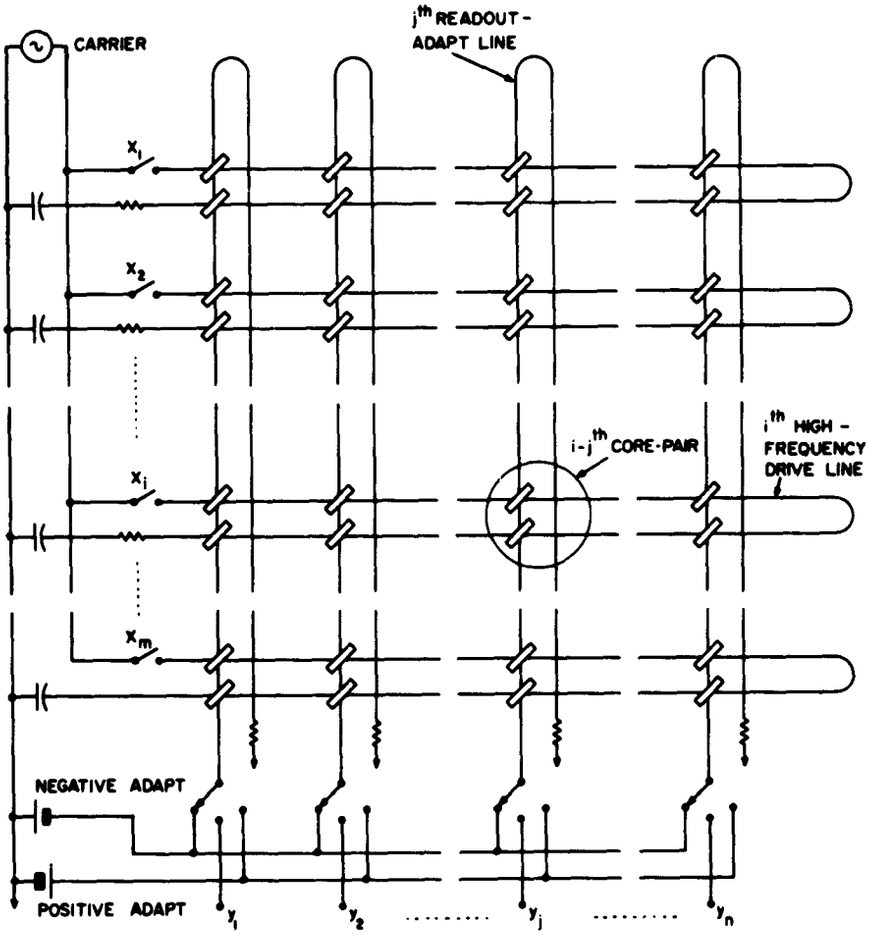


FIG. 11 MATRIX ARRAY FOR COORDINATE ADDRESS SCHEME

On any Y-line, only those stored values are read-out whose X-lines are being driven. Thus, the sum $y_j = \sum_{i=1}^{M} x_i w_{ij}$ ($x_i = 0$ or 1, and w_{ij} is the stored value of the $\underline{i}$-$\underline{j}$th weight), is formed by measuring the output, y_j, on the $\underline{j}$th Y-line, with those X-lines excited which correspond to $x_i = 1$ and those X-lines not excited which correspond to $x_i = 0$. In a random-access, analog-storage memory, the stored value (w_{ij}) of the $\underline{i}$-$\underline{j}$th weight would be read-out by exciting the $\underline{i}$th X-line with high-frequency drive current and reading the second harmonic output voltage across the terminals of the $\underline{j}$th Y-line.

The adaptation rule for $x_i = 0$ or 1, is $\Delta w_{ij} = \delta x_i \text{ sgn } \Delta y_j$, where

Δy_j = the desired change in the value of y_j

The Δw_{ij} are the corresponding changes in the weights w_{ij} that are on the $\underline{j}$th Y-line, which produce Δy_j

δ is the size of the change and equals the magnitude of Δy_j divided by the total number of x_i, $i = 1, 2, \ldots, m$ which equal 1

sgn Δy_j = ± 1 when Δy_j is positive or negative, respectively, or zero when Δy_j is zero.

This rule is often applied to adaptive networks and can be implemented in the following way: Excite only those X-lines for which $x_i = 1$ and excite the $\underline{j}$th Y-line with the polarity of adapt pulse which corresponds to sgn Δy_j. The length of the adapt pulse determines δ.

The coincidence of the high-frequency drive current and the adapt pulse will adapt only those weights in which a change is desired. This allows all weights to be adapted <u>simultaneously</u> according to the above rule. It takes only the duration of the adapt pulse to change all $m \times n$ weights.

A prototype array of such weights is now under construction where $m = 17$ and $n = 33$. Twelve such arrays will constitute the adaptive network of weights in MINOS II, for a total of 6732 weights.

IV LEARNING MACHINE SIMULATION EXPERIMENTS

A. BACKGROUND

The simulation experiments that were described in Quarterly Progress Report 9 are intended to evaluate the performance of different learning machine structures; these experiments have been continued using up to 600 patterns in the training sequence. Certain modifications were introduced in the computer programs to obtain a better comparison between the performance of the integrated and parallel system designs. Preliminary results indicated little difference in the performance of the integrated and parallel structures. Also, there was little difference in the performance of the two parallel systems being evaluated--the majority-logic and the parity systems discussed in Quarterly Progress Report 8. It therefore seemed desirable to concentrate the available resources for simulation on testing the majority-logic system, because if the results indicated the desirability of building the parallel structure, this would be the easier of the two parallel arrangements to implement.

Originally, it was thought that the number of training iterations required on a random pattern set to reduce the number of incorrect responses to zero would provide an adequate criterion for the comparison of system performance. However, since long tails appeared on the learning curves, so that a small number of errors persisted for many iterations before final convergence was achieved, it was considered desirable to compare the whole history of training and learning for the two candidate systems.

B. MODIFICATIONS TO THE SIMULATED INTEGRATED SYSTEM

A typical set of learning curves for the integrated system was presented in Quarterly Progress Report 9; the curves showed the number of correctly identified patterns, uncertain responses, and incorrectly identified patterns, as a function of the number of training iterations performed on a set of 200 random patterns. The response to a pattern was

considered as uncertain when the resulting A-unit vector was equidistant from the desired prototype filter and one or more of the other filters. The relatively large number of uncertainties present was at least partly attributable to the small Hamming distance between the prototype filters in the reduced-scale system studied. It is probable that the reduction in scale tended to bias the results against the integrated system design.

One possibility that was explored as a means of resolving the ambiguous responses was the development, for the prototype filters, of a set of codes which would exhibit the property of having an odd Hamming distance between equidistant code words. Unfortunately, it was shown to be theoretically impossible for such a code structure to exist. As an alternative, the following tie-breaking rule was implemented to resolve the ambiguities:

> Resolve a tie between two or more categories in the association-unit space in favor of the category having the lowest assigned number.

This rule served not only to eliminate the uncertain responses but also to change the learning curve somewhat by correcting fewer patterns (previously the weights had been adapted when an uncertain response occurred). The over-all training time improved slightly and, in the case of 200 random patterns, was reduced from 15 to 14 training iterations of the pattern set. The residual errors--that is, the errors occurring on a test-only phase after each training iteration--are shown in Fig. 12 for random pattern sets of 200, 400, and 600 one-hundred-bit pattern vectors.

C. SIMULATION OF THE PARALLEL MAJORITY-LOGIC SYSTEM

The scaled-down majority-logic system compared 100 input points connected through adjustable weights to sixteen threshold logic units arranged in four groups of four units each, as shown in Fig. 13. The total number of threshold-logic units was chosen to be as close as possible to the number used in the integrated system, although the even number of association units in each set precluded obtaining a true

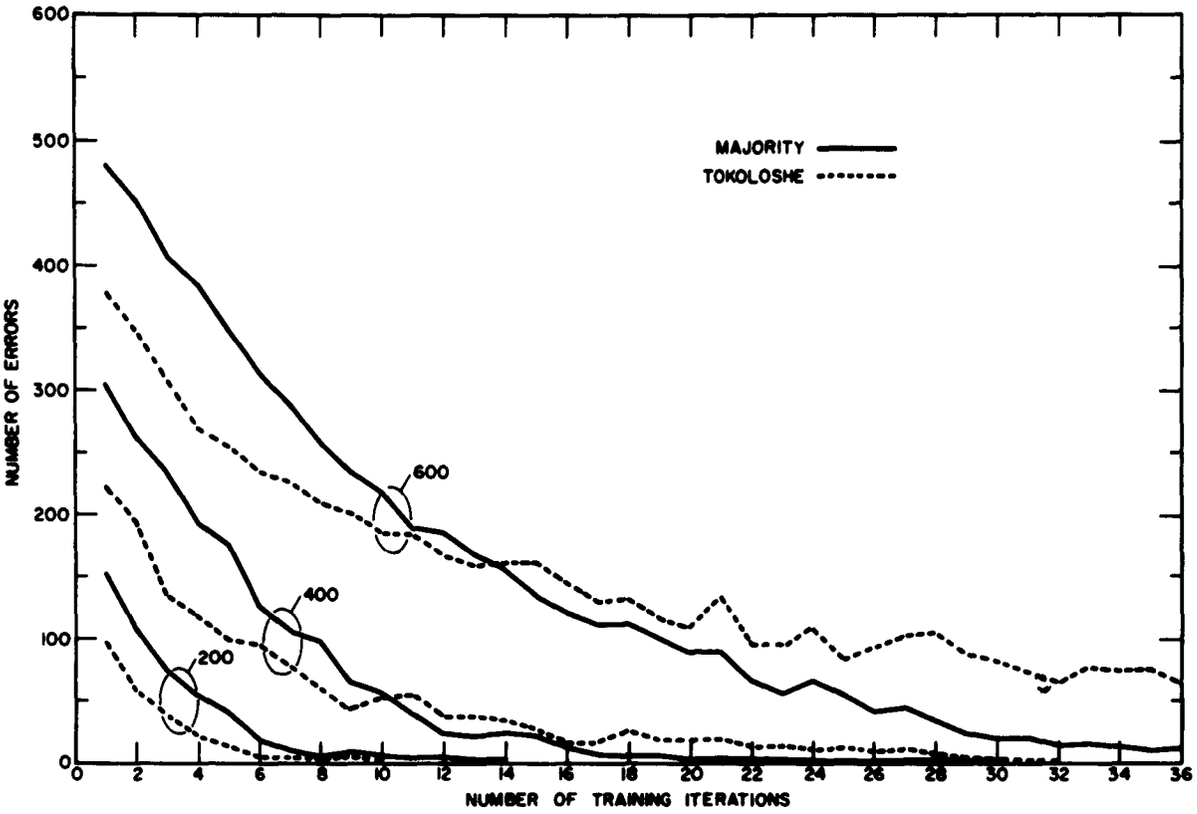


FIG. 12 LEARNING CURVES FOR INTEGRATED AND PARALLEL LEARNING MACHINE STRUCTURES SHOWING RESIDUAL ERRORS AFTER EACH TRAINING ITERATION ON RANDOM PATTERN SETS

majority vote and necessitated the use of the following arbitrary tie-breaking rule:

Majority vote = 0, when zero, one, or two A units are turned on.
Majority vote = 1, when three or four A units are turned on.

The category of a random pattern presented at the inputs of the system was started as a four-bit binary number. Each bit in the parallel output code was trained to respond correctly to an entry in a truth table corresponding to that bit position in the binary number. The simulation experiments showed that a considerable variation occurred in the number of training iterations required for each of the parallel outputs, before

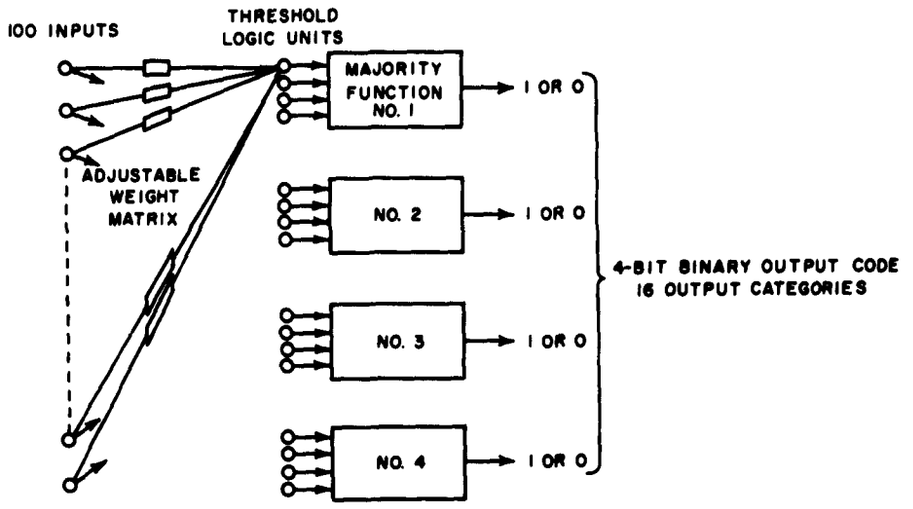


FIG. 13 MAJORITY LOGIC SCHEME USED IN DIGITAL COMPUTER SIMULATION

these converged on the values required for their respective truth tables. For example, in training on the set of 600 patterns, the number of iterations required for convergence of the four respective output units was 35, 44, 33, and 38. In the parallel system a pattern could only be judged to have responded correctly if all four output bits simultaneously gave the desired response for the category of the pattern. If one or more of the output bits was in error for a particular pattern, then the pattern response was judged incorrect.

The curves of the residual errors versus the number of training iterations are shown for comparison on the same graph as the learning curves for the integrated system.

D. COMPARISON OF RESULTS

In all cases the learning curves for the parallel system started off with more residual errors than the integrated system. This might be explained by the fact that fewer incorrect association-unit responses could cause more patterns to be judged in error in the partially trained

parallel system than in the integrated system. An error could have come about if any two out of the four threshold logic units in one output group failed to come on, causing the majority unit to give an output of zero instead of one. On the other hand, four or more of the threshold logic units would have had to be in error to cause an incorrect pattern response in the integrated system.

The residual error curves for the parallel system fell more steeply than the corresponding curves for the integrated system, and showed more of a tendency to converge on a large set of random patterns. A plausible theory put forward to explain this behavior is that once a group of threshold logic units was trained to convergence or near-convergence in the parallel system, those threshold logic units were disturbed less by subsequent training on the few remaining patterns which evoked an incorrect response. In the integrated system, however, it was possible for any of the fifteen threshold logic units to be adapted even in the later stages of the training, thereby changing system behavior to a greater extent on previously learned patterns.

For the foregoing reasons, the parallel structure appears somewhat better suited to the problem of learning a large set of dissimilar patterns such as the ones used in the simulation experiments. Tests were also performed to evaluate the generalization abilities of the two types of system on a small set of equidistant patterns that had noise introduced into the ideal pattern vectors. In this case the integrated system performed slightly better than the parallel system, but the results of these experiments were not sufficiently conclusive to indicate a clear preference for the integrated structure. The generalization properties of the two structures will be re-evaluated when a pattern set becomes available that is more representative of the patterns to be provided by the preprocessor masks.

Additional information and insights were obtained from the simulation experiments pertaining to such factors as the efficiency of various training schemes, the dynamics of weight change and the range of weight values (see, for example, the comments on dynamic range in Sec. II-A).

E. CONCLUSIONS

Of the several forms of learning machine structure that have been simulated, no one system appears to have an appreciable advantage over the others when dealing with random patterns. When the patterns are organized in a manner that is compatible with some particular machine structure, it is assumed that differences will appear. Thus, in deciding which method to use for a practical machine, the absence of other information justifies giving considerable weight to the circuit design problems for each method of hardware implementation. From this point of view, majority logic seems to be easier to implement and easier to trouble-shoot.

V THE ELECTRICAL AND MECHANICAL DESIGN OF THE PREPROCESSOR FOR MINOS II

A. SYSTEM DESIGN REQUIREMENTS

Since the preprocessor is an integral part of the complete machine, its design must be considered together with the over-all functional requirements of MINOS II. The following were the main design criteria:

(1) The machine controls should be arranged to allow the operator to feed in 100-bit patterns manually, and to carry out conveniently other experimental procedures that will sometimes be tedious and repetitive. The machine internal logic should be arranged for self-training--only the patterns (100-bit and graphical) and their required classification will be given by the operator. The input pattern rate should be compatible with standard 16-mm movie film speed (24 different patterns per second).

(2) The automatic training facility requires that a method be available for sequential presentation of patterns--both 100-bit code words and graphical data, along with their classification. Careful consideration was given to the possible use of punched card or punched paper tape systems for the 100-bit patterns, but consultations with suppliers of this type of equipment led to the conclusion that any of these systems would be costly, even on a rental basis, and in any event, existing digital computer equipments would need considerable modification to make use of the ability of our system to operate in parallel. It appears that no suitable, standard, multichannel (approximately 100 channels), parallel, pattern-storage system is available. This difficulty led to the method adopted, in which a permanent record of the patterns can be

stored on standard 16-mm movie film; the same method may be used for presentation of full 10^4-element fine-resolution pictures.

(3) An output display was required from the preprocessor that would permit making comparisons of the code words obtained from various fine-resolution patterns and mask sets. In addition, one eventual goal is to feed a digital computer in real time (with the cooperation of a special parallel-to-sequential coding arrangement being made in an adjacent laboratory by Dr. J. Bliss[2] for a related project) or else to feed a punched-card printer, giving off-line computer input facilities. Care is being taken to keep the two systems as compatible as possible, since this appears to be a way for us and for Dr. Bliss's group to carry out new and useful experiments that could not otherwise be performed. The output display from the preprocessor must also act as an input display for the learning machine when patterns are fed into the learning machine manually. Thus, 110 touch-operated inputs have been provided, each with a corresponding lighted display and pushbutton.

(4) Since the adaptive weight element had not been finally determined, it was decided not to regard this as a design restriction, but to provide as much output power as was reasonably possible, and voltage levels commonly used for transistor-switching circuit inputs.

(5) Cost governed the choice of components except where less expensive components would have degraded the performance significantly.

B. IMPLEMENTATION OF REQUIREMENTS

A pattern can be entered into the preprocessor in one of two ways. First, for manual operation, an electric pencil is stroked over the

"operator's retina," and every square touched by the electric pencil lights up. The squares remain lit until the complete retina is "erased" by means of a single pushbutton. When performing coding-type experiments, the operator must pick out about 55 out of 110 elements, and must be able to correct single errors without having to start writing the pattern over from the beginning. Thus, pushing any lighted square causes it to be extinguished; the element itself is an illuminated pushbutton. Once a pattern has been set up, a permanent record can be made by photographing the separate "bright retina" provided for that purpose. It is not necessary to make the record; the operator can feed in the pattern by operating the "initiate" pushbutton provided on his panel. The "operator's retina" could not be used for the training film, since the low level of illumination makes ambient light relatively disturbing. Also, the illumination intensity is uneven, and the touch-sensitive facility requires a metal ring to be let into the center of each element.

Second, for automatic operation, inputs can be made via 35-mm slide, or 16-mm movie film. The patterns can be graphical data, such as fine-resolution map symbols, or training or test film made from photographing the bright retina. When performing experiments using the 100-bit input code, and feeding these in via a movie film (or 35-mm slide), it is necessary to prevent all but the light from the corresponding 1-percent area of the pattern from affecting the photoconductor. This imposes a fairly severe requirement on the sensitivity of the amplifying devices.

The block diagram of the preprocessor system is shown in Fig. 14. Only one emitter circuit is shown. One of these is behind each photocell. A more detailed discussion of the input structure was given in Quarterly Progress Report 7.

Each photoresistor is illuminated according to the pattern-mask combination, and the resistance of the photo-device changes according to the total integrated incident light. A 1000-cps signal is applied to the photoresistor, which is in turn connected to the input of an emitter-follower, impedance-changing, amplifier stage. This stage is placed just behind its associated photocell to minimize stray pickup effects. The

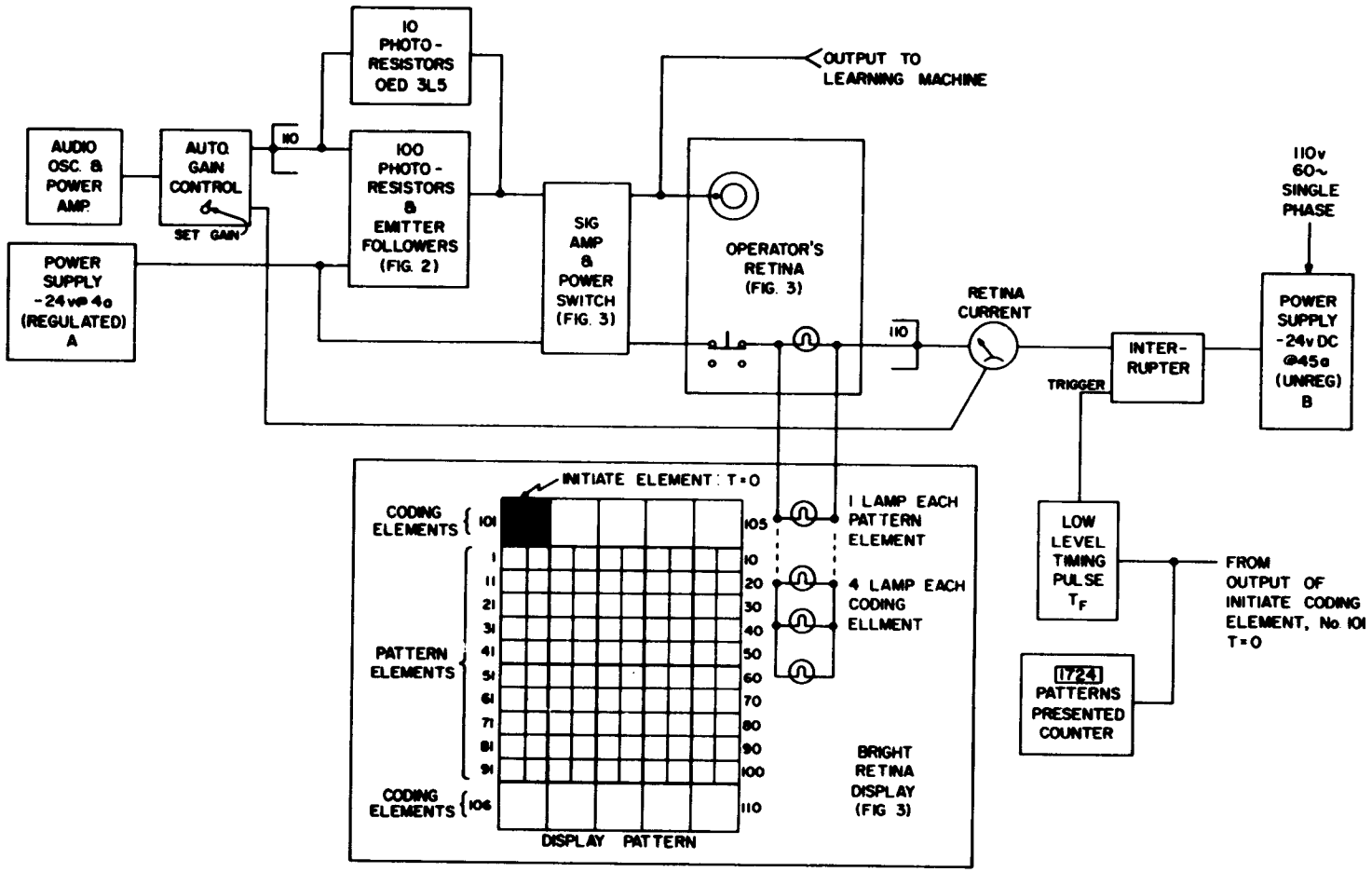
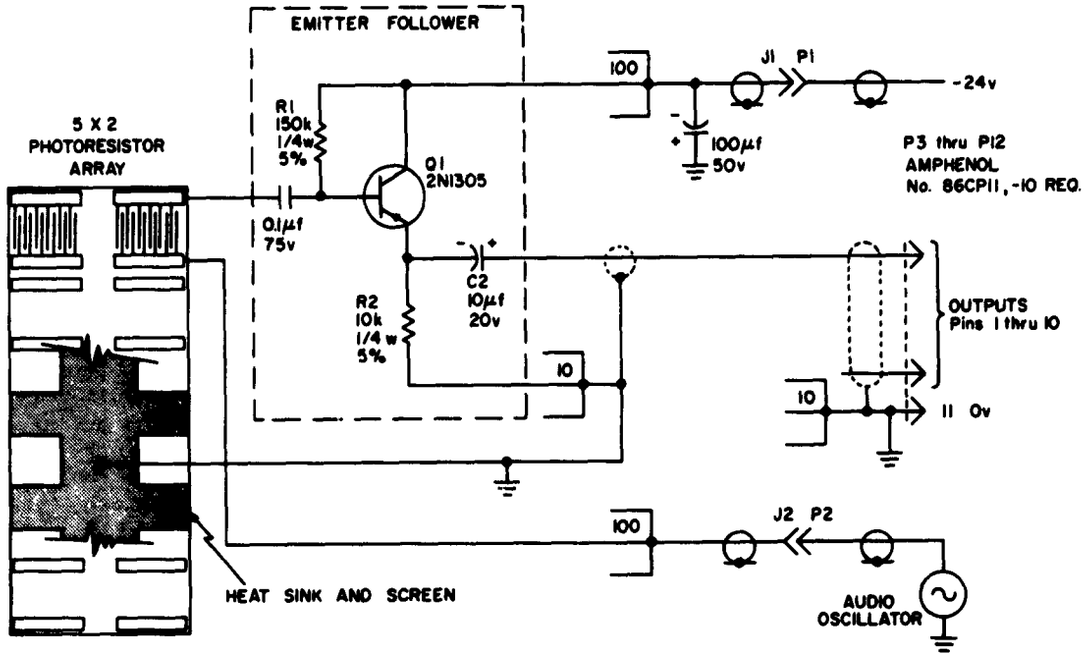


FIG. 14 BLOCK DIAGRAM OF PREPROCESSOR

output of this circuit is connected to a screened cable about 6 feet long, which connects, by means of a plug and socket, into the equipment rack, and into the input of the transistor-and-silicon-controlled-rectifier (SCR) combination. The purpose is to raise the signal level and switch the SCR, to provide the required lamp display and the voltage change at the output terminal. The total retina current will be a measure of the activity of the pattern-mask combination, and it is desirable to maintain approximately half the elements on for every picture. Thus, the retina current will be monitored and used to control the magnitude of the 1000-cps signal to give approximately 50 percent activity, which means constant retina current. The manual gain control shown on the block representing the AGC circuit permits us to have, say, 40 percent or 60 percent activity instead of 50 percent. Once an SCR has been fired, it remains conductive until the load current has been reduced below a certain critical value. This feature provides the "self-locking" property. In order to erase the retina, the interrupter must effectively become an open circuit to reduce the retina current below the striking value.

The only photoresistor that came within the sensitivity, cost, and response-time requirements was a cadmium selenide photoresistor (p. 17 of Quarterly Progress Report 8). Preliminary tests on a standard production type 0E3L5 showed promise, and a suitable quantity of 5 x 2 cell arrays, each cell having an active area approximately 1/2 inch square, was ordered. The layout of one of these arrays is shown in Fig. 15, together with its associated amplifier circuit. The photo device has a high resistance (greater than 100 megohms at 55°C) when dark, and when illuminated its resistance falls typically to approximately 10 kilohms at an illumination of 10 foot candles from a tungsten lamp. Since the illumination level we anticipate being able to produce is much less than this, we must regard the device as operating in the high-impedance region, as far as transistor circuitry is considered. In view of the sensitivity requirements and limited light intensity, it is desirable to use the device to its limit. The limiting factor is the 150-volt rating of the cells.



NOTE: 1. 100 EMITTER FOLLOWER CIRCUITS CONNECTED IN PARALLEL AS SHOWN BY SYMBOL }.

2. NUMERAL IN SYMBOL INDICATES NUMBER OF CIRCUITS IN PARALLEL.

FIG. 15 PREPROCESSOR FRONT-END CIRCUITRY

The transistors for the emitter follower were chosen on the basis of cost (approximately $0.40 each), although the performance characteristics of the mass-produced 2N1305 are adequate. The emitter-follower configuration was chosen since this provides the required high input impedance and low output impedance. The switching characteristics of the circuit should be such that an illuminated cell with the highest value of audio voltage applied should give less than 1-percent output required to fire an SCR, while a fully illuminated cell should give a saturated output, 24 volts peak-to-peak, under the same conditions. This requirement places a restriction upon the operating frequency, since the cell is not purely resistive and has an appreciable parallel capacitive component. In order to fulfill these requirements, a frequency of 1000 cps was chosen. Alternating-current coupling was chosen for reasons of temperature stability, and a certain amount of 60-cps rejection capability.

C. TEST RESULTS

Parts of the system shown on the block diagram (Fig. 14) have been constructed and tested. Since the equipment is mainly a repetition of 110 similar circuits, the variations among circuits are one of the chief properties of interest. The photocells themselves show a variation in illuminated resistance from 1 megohm to 30 kilohms. These measurements were taken with the cells mounted in the preprocessor, using no masks, and some of the observed variation is undoubtedly due to differences in the preprocessor optical system. Large differences will have to be corrected in the electronic system if all elements in the code word are to be equally biased. The mean of the photocells resistance is 224 kilohms taken for 16 arrays--i.e., 160 cells. It is possible to select the best 10 arrays for use in the equipment, but since 10 cells are physically mounted together, the arrays chosen must contain 10 uniformly good cells. A set of measurements was taken of the audio frequency voltages required to fire the SCRs, using the same photocell and emitter follower, with a 1-percent transmission mask. The minimum voltage to fire was 6.5 volts rms, and the maximum was 50 volts. The mean for this parameter is 28.6 volts. The variation of triggering currents for SCRs was measured by connecting a variable dc power supply in series with 1000 ohms, and measuring the voltage across this resistor. The range of currents was from 1.2 milliamperes to 17 milliamperes, with a mean of 8.58 milliamperes.

The equipment has also been set up by adjusting the sensitivity potentiometer connected in the base circuits of the 2N1305 amplifier stages (see Fig. 16) so that all cells in the 110-element array come on between 1.7 and 3.4 volts, rms, of audio frequency signal, with no masks in the system. Further narrowing of this spread will require selective techniques and rewiring of insensitive parts of the circuit to other sensitive parts, to even out the over-all variations. Fortunately, this type of variation, as long as it remains constant with time and normal environmental conditions, should not disturb effective working of the machine, requiring merely a slightly different set of weights from that set which would be required if all circuits were identical.

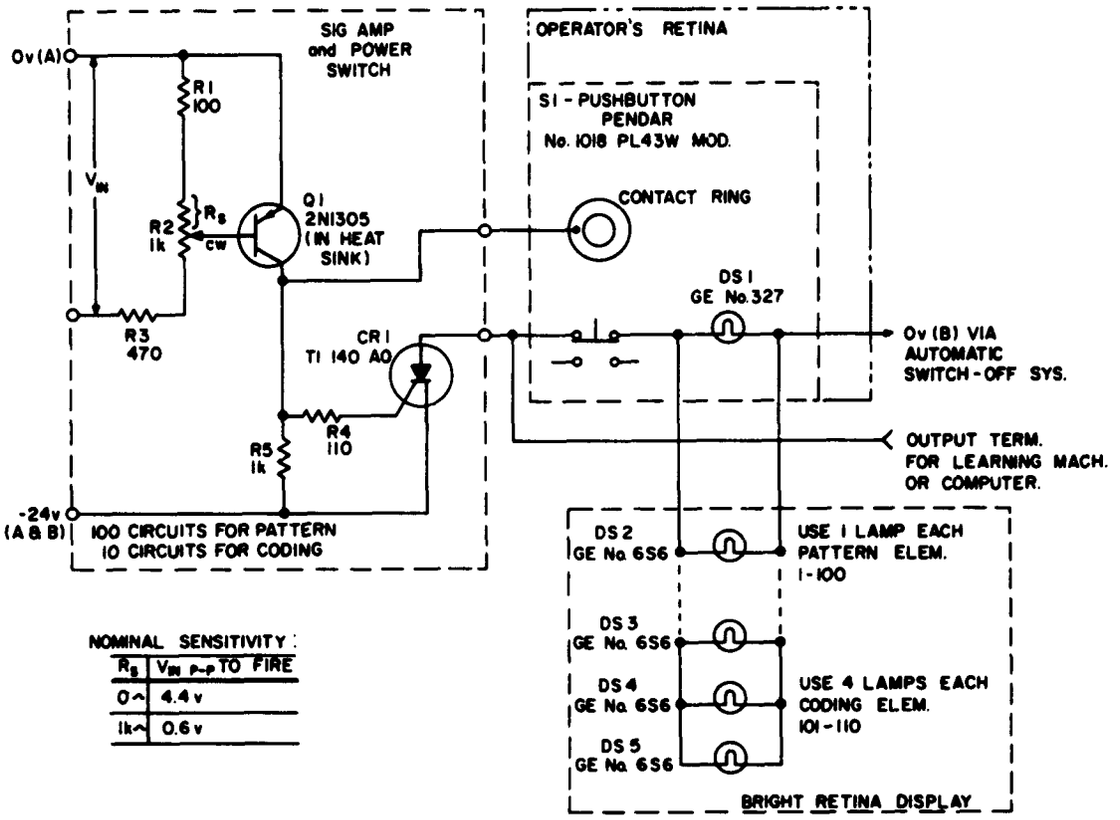


FIG. 16 PREPROCESSOR SIGNAL AMPLIFIER AND POWER SWITCH

The parts of the preprocessor to be constructed next are the power supply suitable for operating all the lamps in the bright retina, the pattern-counting and control circuits, and the automatic threshold control.

VI CONCLUSIONS

The design of MINOS II was determined by system simulation, laboratory experimentation, and construction time and cost estimates resulting therefrom.

It was decided to use 100 replications, each with a 10,000-bit resolution of the optically projected pattern. Each replication would be sampled by its associated mask (one section of a single photographic transparency) and thresholded to provide 100 binary outputs. These outputs would be made available to the adaptive section of MINOS II or other computing equipment. The construction and testing of the preprocessing unit is nearing completion.

The adaptive section of MINOS II will use tape-wound, core-pair weights. There will be 6732 (66 x 102) weights from 100 binary input channels (plus one for the variable threshold and one spare) arranged in six groups of eleven output Threshold Logic Units. Each input is connected to each TLU by one weight. Initially, each group of eleven TLU outputs will be processed according to a majority rule scheme to produce a single binary decision, totalling six such binary outputs for the machine. The machine will be constructed so as to allow the later addition of more complicated variations.

PROGRAM FOR THE INTERVAL 1 DECEMBER 1962 TO 28 FEBRUARY 1963

Twelve arrays of 561 (33 x 17) tape-wound, core-pair weights are to be constructed, tested individually, and assembled in the majority-rule, output-logic system. Transistor-magnetic circuitry will be used to implement the output and increment-decrement circuitry. Vacuum-tube circuitry for providing high-frequency power to the weights was determined mainly by cost considerations.

A set of masks for the preprocessor is being generated and will be tested.

IDENTIFICATION OF KEY TECHNICAL PERSONNEL

(For the Period 1 October to 29 December 1962)

	Hours charged to the Project
Dr. Alfred E. Brain	
Research Physicist, Applied Physics Laboratory (Project Leader)	355
Mr. Harold S. Crafts	
Research Engineer, Applied Physics Laboratory	47
Mr. George E. Forsen	
Research Engineer, Applied Physics Laboratory	369
Mr. David J. Hall	
Research Engineer, Applied Physics Laboratory	375
Miss Marian F. Hirsch	
Research Chemist, Applied Physics Laboratory	38
Mr. Jack W. Machanik	
Research Engineer, Systems Engineering Department	8
Dr. Charles A. Rosen	
Manager, Applied Physics Laboratory	29
Shop and Technicians	1,270
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Editorial	3

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Report No. 10, Quarterly Progress Report 10, 1 September to 30 November 1962, 37 pages, 37 Figs.

Contract DA 36-039 SC-78343, SCL-4087 (18 November 1958), File No. 40001-PM-60-91-91(6500), DA Project 3A99-22-001-02. UNCLASSIFIED report.

An experimental pattern-recognition machine, MINOS II, is to be constructed. The fundamental premise is that the development of inexpensive, adaptive weights will allow their use in quantities sufficient to ensure the practicality of learning machines for real pattern-recognition tasks. Several devices dependent on the electromagnetic or magnetostrictive properties of common magnetic materials or components have been developed and are described. All are compatible

UNCLASSIFIED

1. Graphical Data processing
2. Contract DA 36-039 SC 78343
3. Pattern recognition
4. Learning Machines
5. Inexpensive, adaptive weights
6. Majority-rule coding
7. System and circuitry requirements for MINOS II

I Graphical Data Processing Research Study and Experimental Investigation

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